

WHAT IS CLAIMED IS:

1 1. An apparatus capable of processing a multimedia digital
2 bitstream, said apparatus comprising:

3 a processing chain comprising a plurality of media processors
4 wherein each of said plurality of media processors is capable of
5 processing a portion of said multimedia digital bitstream

6 wherein each of said plurality of media processors is capable
7 of splitting said portion of said multimedia digital bitstream into
8 a primary bitstream and a secondary bitstream, and capable of
9 processing said primary bitstream, and capable of merging a
10 processed primary bitstream with said secondary bitstream.

1 2. The apparatus as claimed in Claim 1 wherein the number of
2 said plurality of media processors may vary from two to N, where N
3 is an integer number greater than two.

1 3. The apparatus as claimed in Claim 1 wherein said
2 multimedia digital bitstream comprises a high definition digital
3 video signal.

1 4. The apparatus as claimed in Claim 1 wherein each of said
2 plurality of media processors comprises a bitrate transcoder unit
3 capable of transcoding a portion of said multimedia digital
4 bitstream.

1 5. The apparatus as claimed in Claim 4 wherein said bitrate
2 transcoder unit comprises a split unit, a BRT' transcoder, and a
3 merge unit.

1 6. The apparatus as claimed in Claim 4 wherein said bitrate
2 transcoder unit comprises an output component that is capable of
3 generating empty data packets and adding said empty data packets to
4 the output of said bitrate transcoder unit.

1 7. The apparatus as claimed in Claim 6 further comprising a
2 clock control circuit in an output component of a last bitrate
3 transcoder unit that is located at an output end of said processing
4 chain, wherein said clock control circuit is capable of adjusting a
5 clock rate of an output of said last bitrate transcoder unit in
6 said processing chain.

1 8. The apparatus as claimed in Claim 1 wherein said
2 processing chain further comprises:

3 an input block coupled to a first media processor in said
4 processing chain, wherein said input block is capable of receiving
5 multimedia data in real time from one of: a computer file, a
6 bitpump, and a radio frequency front end; and

7 an output block coupled to a last media processor in said
8 processing chain, wherein said output block is capable of
9 outputting multimedia data in real time in one of: a computer file
10 format, and a transport stream format.

1 9. A television unit comprising an apparatus capable of
2 processing a multimedia digital bitstream, said apparatus
3 comprising:

4 a processing chain comprising a plurality of media processors
5 wherein each of said plurality of media processors is capable of
6 processing a portion of said multimedia digital bitstream

7 wherein each of said plurality of media processors is capable
8 of splitting said portion of said multimedia digital bitstream into
9 a primary bitstream and a secondary bitstream, and capable of
10 processing said primary bitstream, and capable of merging a
11 processed primary bitstream with said secondary bitstream.

1 10. The television unit as claimed in Claim 9 wherein the
2 number of said plurality of media processors may vary from two to
3 N, where N is an integer number greater than two.

1 11. The television unit as claimed in Claim 9 wherein said
2 multimedia digital bitstream comprises a high definition digital
3 video signal.

1 12. The television unit as claimed in Claim 9 wherein each of
2 said plurality of media processors comprises a bitrate transcoder
3 unit capable of transcoding a portion of said multimedia digital
4 bitstream.

1 13. The television unit as claimed in Claim 12 wherein said
2 bitrate transcoder unit comprises a split unit, a BRT' transcoder,
3 and a merge unit.

1 14. The television unit as claimed in Claim 12 wherein said
2 bitrate transcoder unit comprises an output component that is
3 capable of generating empty data packets and adding said empty data
4 packets to the output of said bitrate transcoder unit.

1 15. The television unit as claimed in Claim 14 further
2 comprising a clock control circuit in an output component of a last
3 bitrate transcoder unit that is located at an output end of said
4 processing chain, wherein said clock control circuit is capable of
5 adjusting a clock rate of an output of said last bitrate transcoder
6 unit in said processing chain.

1 16. The television unit as claimed in Claim 9 wherein said
2 processing chain further comprises:

3 an input block coupled to a first media processor in said
4 processing chain, wherein said input block is capable of receiving
5 multimedia data in real time from one of: a computer file, a
6 bitpump, and a radio frequency front end; and

7 an output block coupled to a last media processor in said
8 processing chain, wherein said output block is capable of
9 outputting multimedia data in real time in one of: a computer file
10 format, and a transport stream format.

1 17. A method for processing a multimedia digital bitstream
2 comprising the steps of:

3 processing a portion of said multimedia digital bitstream in
4 each of a plurality of media processors of a processing chain;

5 wherein each of said plurality of media processors executes
6 the steps of:

7 splitting said portion of said multimedia digital bitstream
8 into a primary bitstream and a secondary bitstream;
9 processing said primary bitstream; and
10 merging a processed primary bitstream with said secondary
11 bitstream.

12 18. The method for processing a multimedia digital bitstream as
13 claimed in Claim 14 wherein the step of processing said primary
14 bitstream comprises the step of:

15 transcoding said primary bitstream in a bitrate transcoder
16 unit.

1 19. The method for processing a multimedia digital bitstream
2 as claimed in Claim 18 further comprising the steps of:
3 generating empty data packets in an output component of said
4 bitrate transcoder unit; and
5 adding said empty data packets to the output of said bitrate
6 transcoder unit.

1 20. The method for processing a multimedia digital bitstream
2 as claimed in Claim 19 further comprising the step of:
3 adjusting a clock rate of an output of at least one bitrate
4 transcoder unit in said processing chain with a clock control
5 circuit.